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, Issue: 1 , Jan 1987  
Pages:48 - 59[\[Abstract\]](#) [\[PDF Full-Text \(1160KB\)\]](#) **IEEE JNL****2 Comments on 'Numerical analysis of H-plane waveguide junctions by combination of finite and boundary elements'***Leviatan, Y.; Sheaffer, G.S.;*Microwave Theory and Techniques, IEEE Transactions on , Volume: 37  
, Issue: 4 , April 1989  
Pages:805 - 806[\[Abstract\]](#) [\[PDF Full-Text \(136KB\)\]](#) **IEEE JNL****3 Composite inductive posts in waveguide-a multifilament analysis***Sheaffer, G.S.; Leviatan, Y.;*Microwave Theory and Techniques, IEEE Transactions on , Volume: 36  
, Issue: 4 , April 1988  
Pages:779 - 783[\[Abstract\]](#) [\[PDF Full-Text \(384KB\)\]](#) **IEEE JNL****4 The cache injection/cofetch architecture: initial performance evaluation***Milutinovic, V.; Milenkovic, A.; Sheaffer, G.;*Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, 1997. MASCOTS '97., Proceedings Fifth International Symposium on , 12-15 Jan. 1997  
Pages:63 - 64[\[Abstract\]](#) [\[PDF Full-Text \(196KB\)\]](#) **IEEE CNF****5 Performance and hardware complexity tradeoffs in designing multithreaded architectures***Bekerman, M.; Mendelson, A.; Sheaffer, G.;*Parallel Architectures and Compilation Techniques, 1996., Proceedings of the 1996 Conference on , 20-23 Oct. 1996  
Pages:24 - 34[\[Abstract\]](#) [\[PDF Full-Text \(1128KB\)\]](#) **IEEE CNF**

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*Masselos, K.; Cathoor, F.; Kakarudas, A.; Goutis, C.E.; De Man, H.;*  
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*Truslove, K.C.E.;*  
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**4 Engineering data re-use at JPL: promise and perils**

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**5 LSI design toward 2010 and low-power technology**

*Sakurai, T.;*  
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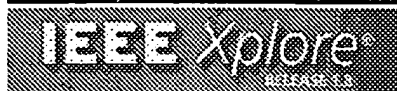
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*Cosatto, E.; Craf, H.P.;*  
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#### 2 Design of bit manipulation accelerator for communication DSP

*Suk Hyun Yoon; Sug Hyun Jeong; Myung Hoon Sunwoo;*  
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*Vassiliadis, S.; Hakkennes, E.A.; Wong, J.S.S.M.; Pechanek, G.G.;*  
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*Watson, C.R.; Cavaiuolo, M.;*  
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